CS613 Spring 2012 Exam 1 practice -- answers

1. A program executes in 10 sec on a particular computer. The computer's branch-processing subsystem is upgraded so that branch instructions execute twice as fast as before. After the upgrade, the original program runs in 8 sec. What fraction of the program's instructions is branch instructions?

   From Amdahl's Law, 8 = 10 (1-x + x/2) → *x = 0.4*

2. You are evaluating two 'C' compilers, A and B, for your computer. You compile the same test program using each compiler. The compiled code from compiler A has an instruction count of 1000_{10} instructions, and average CPI of 2. The compiled code from compiler B has an instruction count of 1200_{10} instructions. When you run the two programs, you find that the CPU time for the two versions is equal. What is the average CPI for the code compiled with compiler B?

   1000 x 2 = 1200 x CPI_B → $CPI_B = 5/3$

3. A data word is stored by a MIPS processor at memory address 1000_{10}. What the memory address of the least-significant byte of the data word?

   MIPS is "big-endien" and memory words occupy 4 bytes so the least-significant byte is at address 1003

4. Write a MIPS code segment for the 'C' statement:
   A = 5 + B[C]
   Assume that A is in $s0, the base address of B is in $s7, and the address of the memory variable C is in $t3.

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lw   $t4, 0($t3)        # $t4 ← C
sll  $t4, $t4, 2        # $t4 ← 4 x $t4
add $t5, $t4, $s7       # $t5 now contains the address of B[C]
lw   $t6, 0($t5)        # $t6 ← B[C]
addi  $s0, $t6, 5       # A = 5 + B[C]
```

5. Encode the MIPS instruction:
   addi $s1, $s2, -17_{16}
   Show the contents of each field in binary.

   Note that you needed to convert the immediate data to 2's complement form
   00 1000 | 1 0010 | 1 0001 | 1111 1111 1110 1001

6. Encode the MIPS instruction:
   lw $s3, 65_{10}($t0)
   Show the contents of each field in hexadecimal.

   23 | 8 | 13 | 41 hex

7. Encode the MIPS instruction:
   bne $s1, $s2, L1
   where the label L1 refers to memory address 1000_{10} and the bne instruction is located at memory address 500_{10}. Show the contents of each field in binary.

   The offset is 1000 – (500 + 4) = 496_{10}
   So the answer is: 00 0101 | 1 0001 | 1 0010 | 0000 0000 0111 1100

8. Encode the MIPS instruction:

   j L2

   where the Jump instruction is located at address 12345678_{16} and the label L2 refers to address 76543210_{16}. Show the contents of each field in hexadecimal.

   Target /4 = 01 1101 1001 0101 0000 1100 1000 0100
   Dropping h/o 4 bits gives 01 1001 0101 0000 1100 1000 0100 = 1950C84 hex
   So the answer: 2 | 1950C84 hex

   Since the instruction attempts to jump outside of the current page of memory, this instruction might result in an assember error, so I also accepted the answer that the jump could not be encoded.