CS613 Spring 2012 Exam 1 Name _Solutions_______________

Show all work. You may leave numeric answers in the form of a fraction.

1. (10 pts) Given two processors, A and B. For a given program, the CPI of A is 4.0 and the CPI of B is 5.0. A's clock frequency is 4Ghz and B's clock frequency is 2GHz. If the program's execution time on A is 10msec, what is the execution time on B?

Time = IC x CPI / clock_freq

10ms = IC x 4 / 4Ghz

IC = 10 x 10^6

TimeB = 10 x 10^6 x 5 / 2x10^9

= 25ms

2. (5 pts) You have a RISC processor and a CISC processor. One has a higher clock frequency than the other. Which one would you expect to have the higher clock frequency? Explain your answer.

The maximum frequency of the processor clock is governed by the complexity of the operations that have to be one in a single clock cycle. Since all we know is that one processor is RISC and one is CISC, we have to think about which one of those would be most likely to have the least complex operations. That would make RISC the better answer.

3. (10 pts) A program's CPU time is 10 seconds on a particular computer. The computer's memory unit is modified; all other parts of the computer are unchanged. After the modification, the program runs in 5 seconds. If 20% of the program's executed instructions are memory-reference instructions, calculate the factor by which the memory speed was increased.

This is an Amdahl's Law problem. According to the problem statement, 80% of the instructions are not affected by the enhancement, so we would never be able to reduce the execution time below 8 seconds, thus, the problem statement is impossible. I gave credit if you attempted to apply Amdahl's Law to the problem. I gave extra credit it you stated that the solution was impossible. I allowed extra credit for recognizing that the problem was stated in terms of the fraction of executed instructions, not the fraction of execution time.

4. (12 pts) Write MIPS assembly language code for the C language instruction:

   A = B[C] + B[5]

   where the address of B[5] is in $s0, the address of C is in $s1, and the result (A) is to be placed in $s2. All variables are word variables.

   This problem is almost exactly like the one we did before, except that instead of the base address of B, I gave you the address of B[5]. You needed to note that the base address of B would be the address of B[5] – 20.

```
lw      $t1, 0($s0)     # load B[5] to $t1
lw      $t2, 0($s1)     # load C to $t2
sll     $t2, $t2, 2     # $t2 = C*4
addi    $s0, $s0, -2010         # $s0 = address of B[5] – 20 = Base address of B
add     $t3, $t2, $s0   # $t3 = address of B[C]
lw      $t4, 0($t3)     # $t4 = B[C]
add     $s2, $t1, $t4   # A = B[C] + B[5]
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5. (8 pts) Encode the following MIPS32 instruction. Show the contents of each individual field in hexadecimal. Show the correct number of hexadecimal digits to represent all bits in the field.

   and $s0, $t1, $t3

   00 | 09 | 0B | 10 | 00 | 24

6. (8 pts) Encode the following MIPS instruction. Show the contents of each individual field in hexadecimal. Show the correct number of hexadecimal digits to represent all bits in the field.

   addi $s1, $s2, -50_{10}

   $-50_{10} = -(0000\ 0000\ 0011\ 0010)_2 = (1111\ 1111\ 1100\ 1110)_{2's} \rightarrow (FFCE)_{16}$

   08 | 12 | 11 | FFCE

7. (8 pts) Encode the following MIPS instruction. Show the contents of each individual field in hexadecimal. Show the correct number of hexadecimal digits to represent all bits in the field.

   sw $s3, -22_{10}($t4)

   $-22_{10} = -(0000\ 0000\ 0001\ 0110)_2 = (1111\ 1111\ 1110\ 1010)_{2's} \rightarrow (FFEA)_{16}$

   2B | 0C | 13 | FFEA

8. (8 pts) Encode the following MIPS instruction. Show the correct number of hexadecimal digits to represent all bits in the field.

beq $t1, $t2, L1

where the label L1 refers to memory address 200_{10} and the beq instruction is located at memory address 500_{10}. Show the contents of each field in binary.

$200_{10} = 504 + 4 \times offset \rightarrow offset = -76_{10} \rightarrow (FFB4)_{16}$

04 | 09 | 0A | FFB4

9. (8 pts) Encode the MIPS instruction:

j L2

where the Jump instruction is located at address $7AF13440_{16}$ and the label L2 refers to address $7AF12440_{16}$. Show the contents of each field in hexadecimal.

2 | 2BC4910

10. (8 pts) Write the MIPS32 assembly-language statement that would be encoded as:

0010 0010 0101 0001 1111 1111 1110 1010

addi $s1, $s2, -2210

11. (5 pts) Write an expression for the limit on the overall speedup that could be achieved by speeding up one component of a processor.

See notes

12. (5 pts) With all other factors equal, which would you expect to result in a lower CPI: a 2-processor machine or a 3-address processor? Explain your answer.

<not graded – error in problem statement>

13. (3 pts) Explain what we mean by "Big-Endian" as opposed to "Little-Endian". Which of the two approaches is used in MIPS?

see notes

14. (2 pts) Explain what is meant when we refer to MIPS as a "load/store architecture".

All memory access is via load and store instructions