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Chapter 6:
Registers and Counters

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4-bit register

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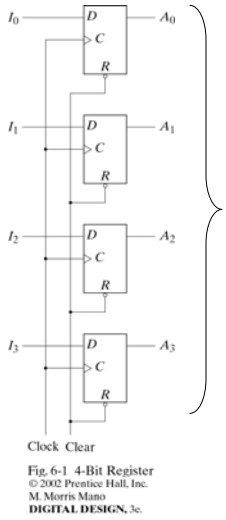
Parallel Input



Parallel Output

Fig. 6-1 4-Bit Register
© 2002 Prentice Hall, Inc.
M. Morris Mano
DIGITAL DESIGN, 3e.

Notice that the register will load from the inputs on every clock pulse

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A more sophisticated register

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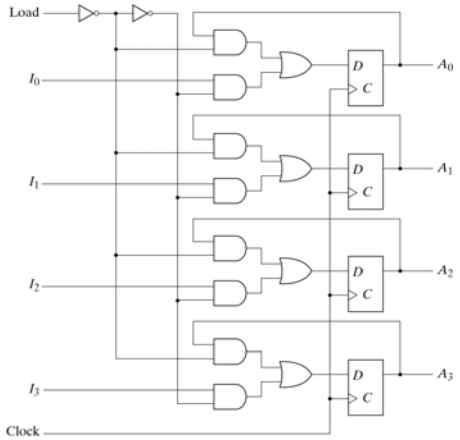

Fig. 6-2 4-Bit Register with Parallel Load

If "Load" =1, the register will load from the inputs

Otherwise, it will hold the stored value

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Serial versus parallel

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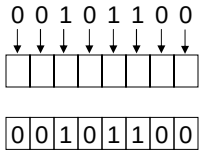
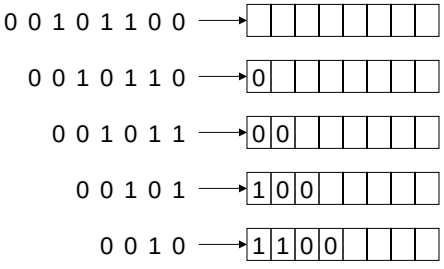
Parallel load



After clock pulse 1

Serial load



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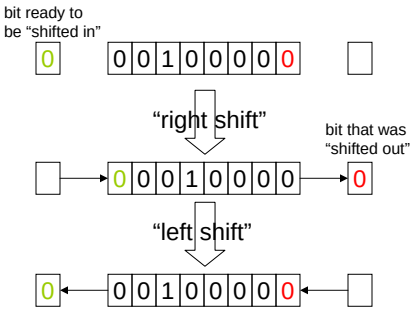
Shift registers

The idea



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4-bit shift register

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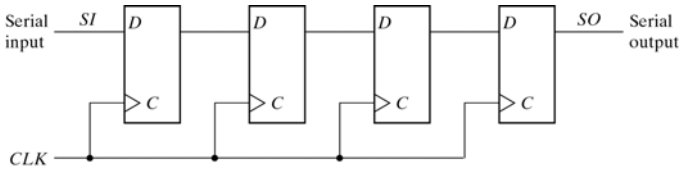

Fig. 6-3 4-Bit Shift Register

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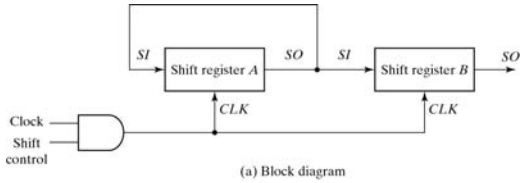
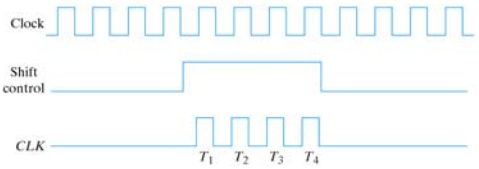
Serial transfer



(a) Block diagram



(b) Timing diagram

Fig. 6-4 Serial Transfer from Register *A* to register *B*

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A serial adder

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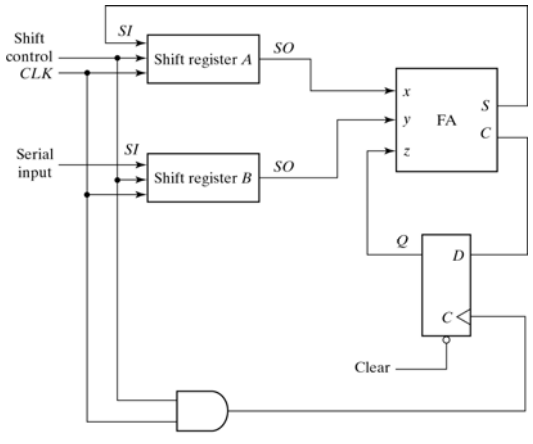

Fig. 6-5 Serial Adder

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Mano's Universal Shift Register

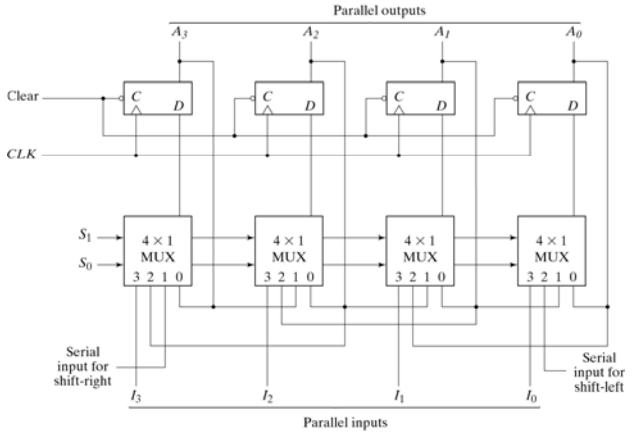

Fig. 6-7 4-Bit Universal Shift Register

mode control

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Operation Diagrams

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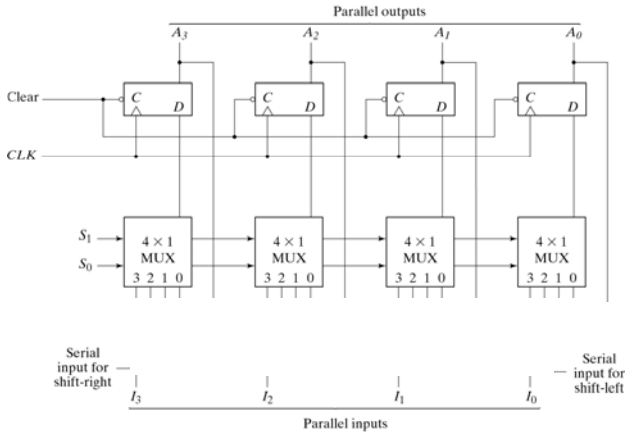

Fig. 6-7 4-Bit Universal Shift Register

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Active lines for Parallel Load

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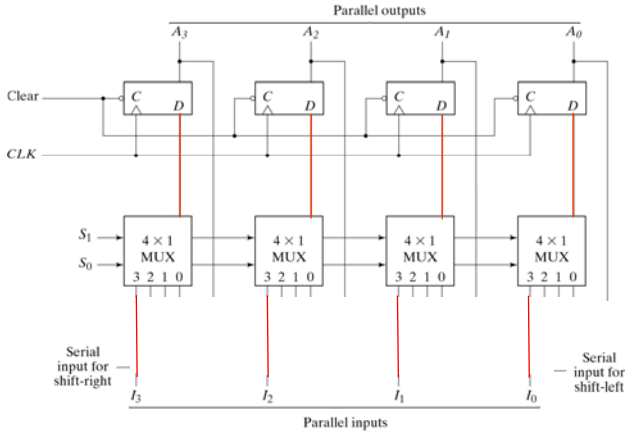

Fig. 6-7 4-Bit Universal Shift Register

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Active lines for No change

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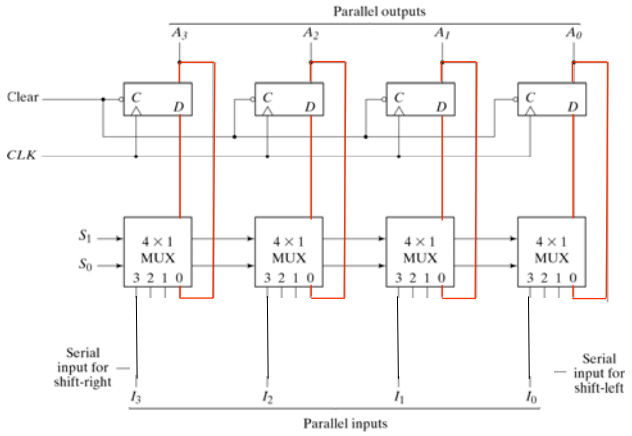

Fig. 6-7 4-Bit Universal Shift Register

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Active lines for Shift Right

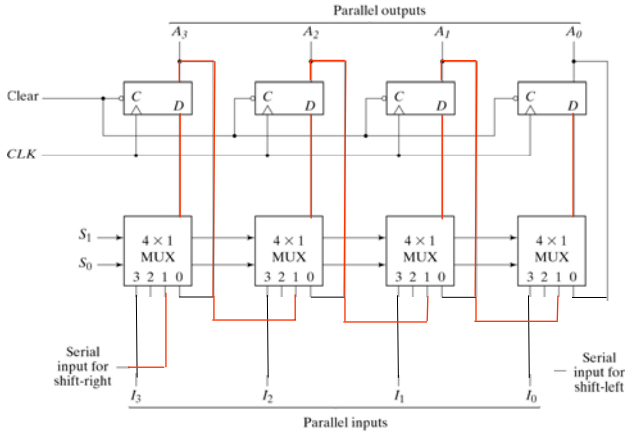

Fig. 6-7 4-Bit Universal Shift Register

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

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Active lines for Shift Left

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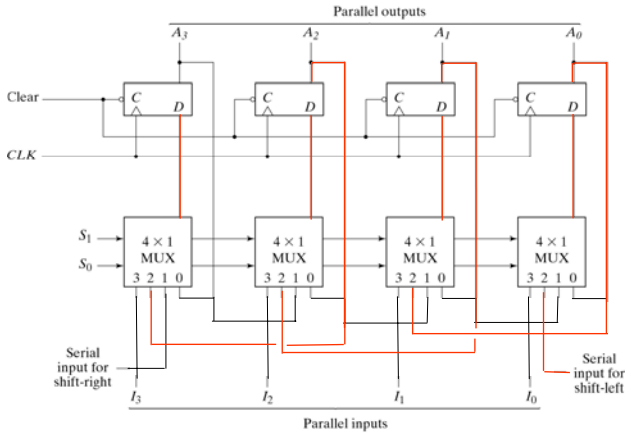


Fig. 6-7 4-Bit Universal Shift Register

S1	S0	Operation
0	0	no change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

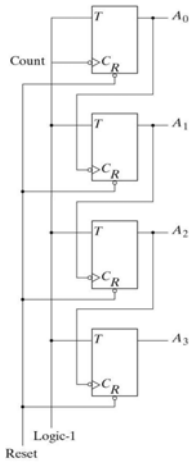
Counters

A Binary Ripple Counter

In a ripple counter, the clock (count) pulse is applied to the first stage only. The change in stage "n" triggers the clock pulse for stage "n+1"

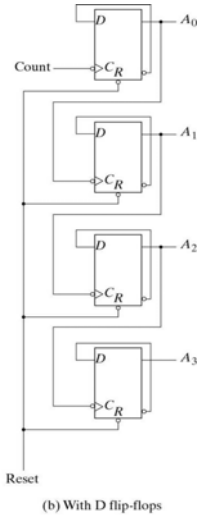
Note that in this design, the FF's are triggered by a 1->0 transition on the clock input

	A3	A2	A1	A0
Reset	0	0	0	0
count 0->1	0	0	0	0
count 1->0	0	0	0	1
count 0->1	0	0	0	1
count 1->0	0	0	1	0
count 0->1	0	0	1	0
count 1->0	0	0	1	1



(a) With T flip-flops

A Binary Ripple Counter



(b) With D flip-flops

	D3	A3	D2	A2	D1	A1	D0	A0
Reset	1	0	1	0	1	0	1	0
count 0->1	1	0	1	0	1	0	1	0
count 1->0	1	0	1	0	1	0	0	1
count 0->1	1	0	1	0	1	0	0	1
count 1->0	1	0	1	0	0	1	1	0

Note that in this design, the FF's are triggered by a 1->0 transition on the clock input

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Decade Ripple Counter

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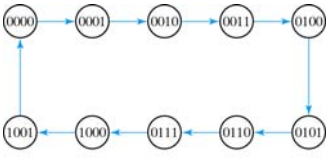

Fig. 6-9 State Diagram of a Decimal BCD-Counter

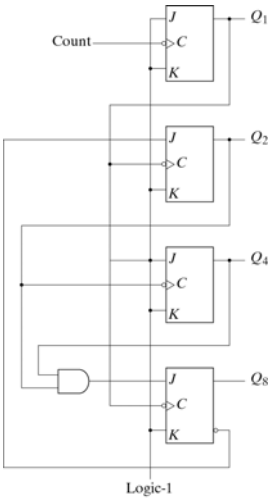

Fig. 6-10 BCD Ripple Counter

3-decade ripple counter

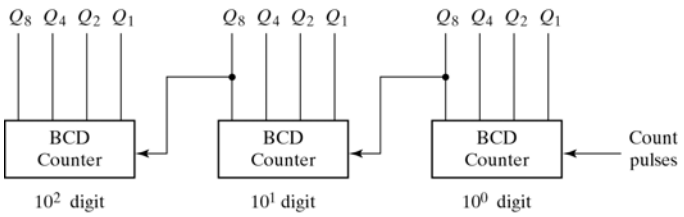

Fig. 6-11 Block Diagram of a Three-Decade Decimal BCD Counter

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Synchronous Counters

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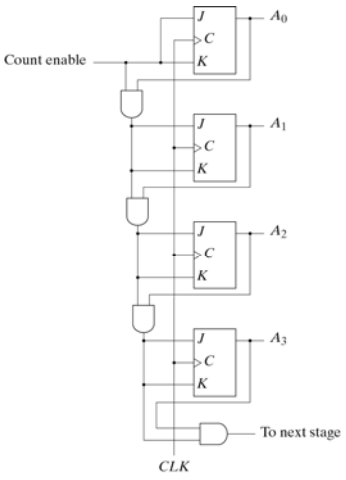

Fig. 6-12 4-Bit Synchronous Binary Counter

In a synchronous counter the clock (count) pulse is applied to all stages at once

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Up-Down Counter

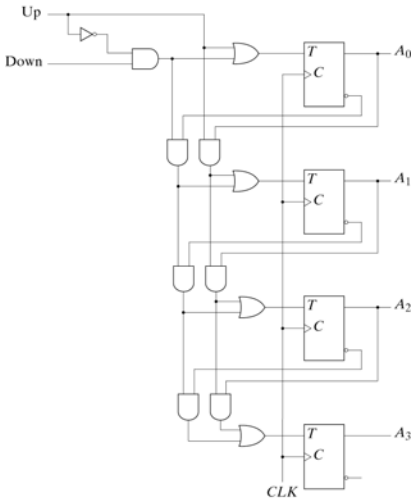

Fig. 6-13 4-Bit Up-Down Binary Counter

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Ring counters

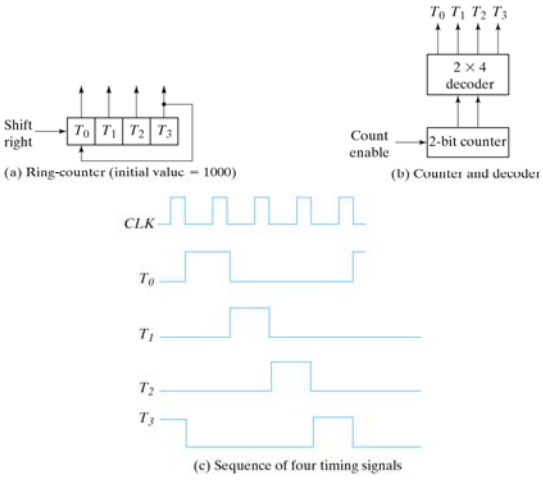

Fig. 6-17 Generation of Timing Signals