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Chapter 5:
Synchronous Sequential Logic

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The idea of a sequential circuit

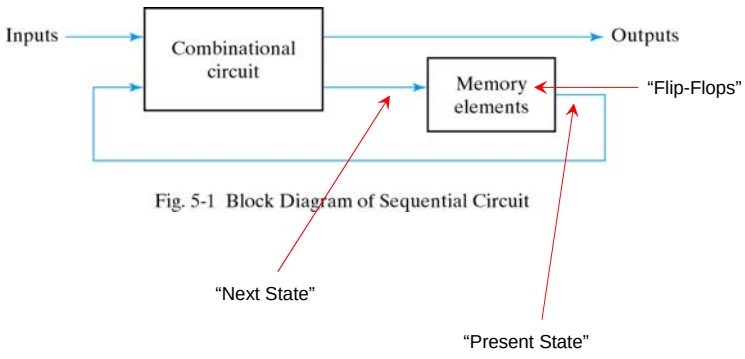
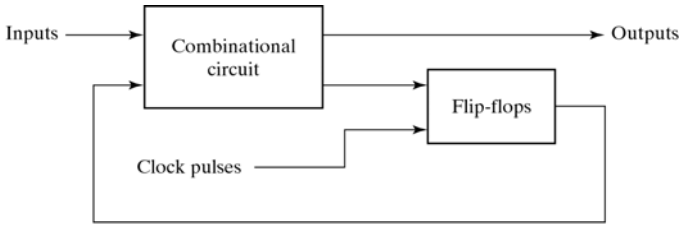


Fig. 5-1 Block Diagram of Sequential Circuit

Synchronous sequential circuits



(a) Block diagram

(b) Timing diagram of clock pulses

Fig. 5-2 Synchronous Clocked Sequential Circuit

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An example flip-flop

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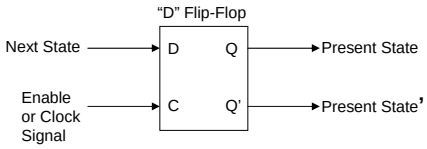

Time

Next State Q(t+1)	Enable	Present State Q(t)
1	0	?
1	1	1
.	.	.
.	.	.
whatever	0	1
.	.	.
.	.	.
0	0	1
0	1	0

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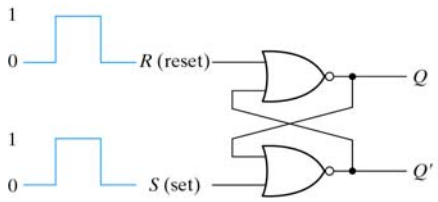
Building Flip-Flops

The heart of a flip-flop is a "latch" circuit



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after $S = 1, R = 0$)
0	1	0	1	
0	0	0	1	(after $S = 0, R = 1$)
1	1	0	0	

(b) Function table

Fig. 5-3 *SR* Latch with NOR Gates

Can also do this with NAND's – see text

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How a latch holds a value

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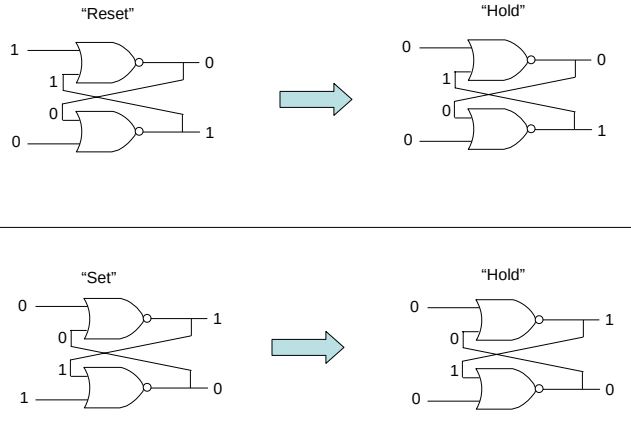

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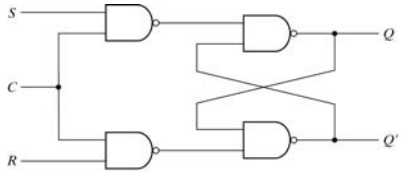
An S-R Flip-Flop



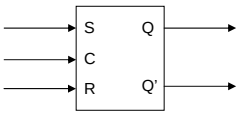
(a) Logic diagram

C	S	R	Next state of Q
0	X	X	No change
1	0	0	No change
1	0	1	Q = 0; Reset state
1	1	0	Q = 1; set state
1	1	1	Indeterminate

(b) Function table

Fig. 5-5 SR Latch with Control Input

Symbol



Characteristic Table

```
S R    Q(t+1)
------------
0 0     Q(t)
0 1      0      "Reset"
1 0      1      "Set"
1 1      Not allowed
```

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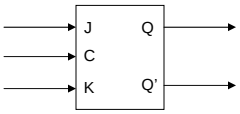
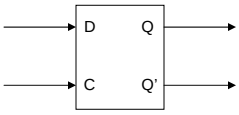
J-K Flip-Flop



Characteristic Table

```
J K    Q(t+1)
------------
0 0     Q(t)
0 1      0      "Reset"
1 0      1      "Set"
1 1     Q'(t)   "Complement"
```

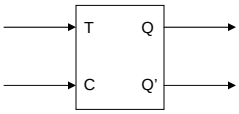
D Flip-Flop



Characteristic Table

D	Q(t+1)
0	0
1	1

T (“Toggle”) Flip-Flop



Characteristic Table

T	Q(t+1)
0	Q(t)
1	Q’(t)

Master-Slave Flip-Flop

We often want to be able to read a stable Present State at the same time we are changing the Next State. We can do this by cascading two latches.

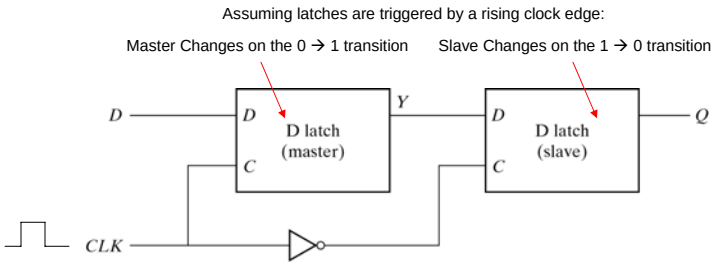


Fig. 5-9 Master-Slave *D* Flip-Flop

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Analyzing Sequential Circuits

Example Circuit

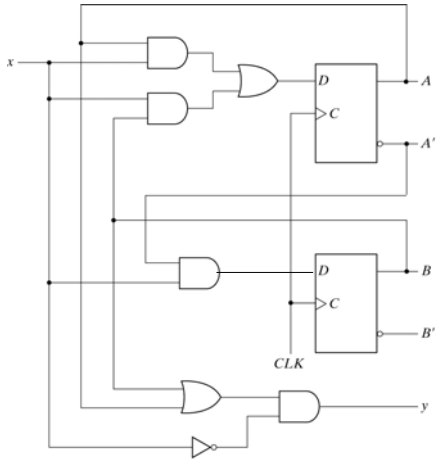

Fig. 5-15 Example of Sequential Circuit

Note:
The "state" of this circuit is the output of the two flip-flops: AB

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Flip-Flop Input Equations

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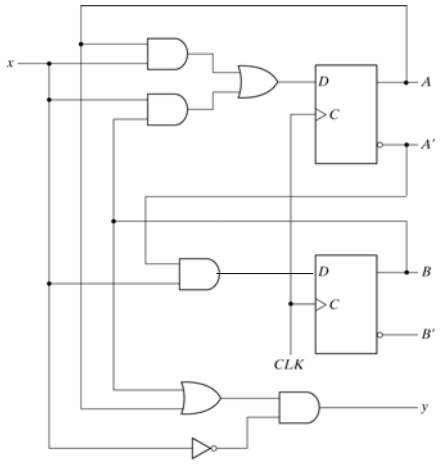

Fig. 5-15 Example of Sequential Circuit

$D_A = A(t)x(t) + B(t)x(t)$

$D_B = A'(t)x(t)$

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State Equations

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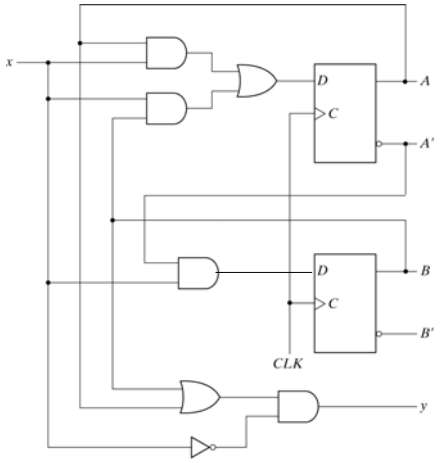

Fig. 5-15 Example of Sequential Circuit

The State Equations specify the next state of the circuit as a function of the present state and inputs.

Because these are D FF's, the next state is equal to the FF inputs

A(t+1) = A(t)x(t) + B(t)x(t)

B(t+1) = A'(t)x(t)

Usually, we drop the "(t)":

A(t+1) = xA + xB

B(t+1) = A'x

Output:
y = (A+B)x'

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State Table

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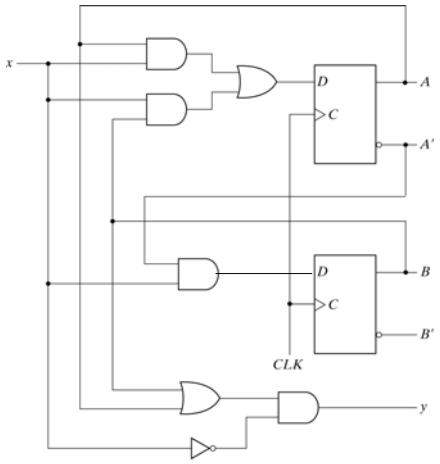

Fig. 5-15 Example of Sequential Circuit

A(t+1) = xA + xB

B(t+1) = A'x

y = (A+B)x'

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

Also note alternate form of the State Table: Table 5.3 in text

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State Diagram

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

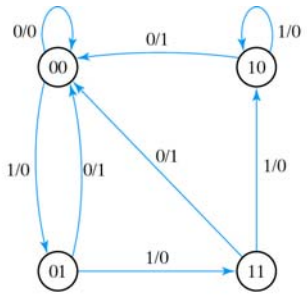

Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

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State Diagram

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Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	1
0	1	1	1	1	0
1	**0**	**0**	**0**	**0**	**1**
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	1	0	0

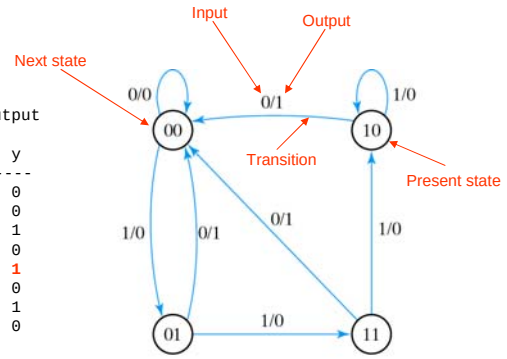

Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

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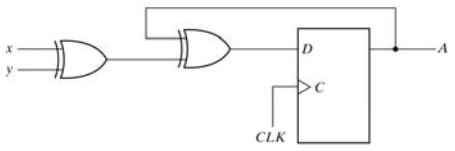
Sequential circuit analysis (continued)

Another D-FF example

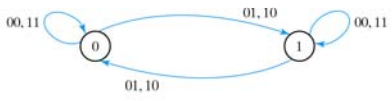


(a) Circuit diagram

Present state	Inputs		Next state
A	x	y	A
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

(b) State table

D = x XOR y XOR A



(c) State diagram

Fig. 5-17 Sequential Circuit with *D* Flip-Flop

Note that since the circuit output is the state, we do not need to show the output value on the transition lines.

JK-FF Example

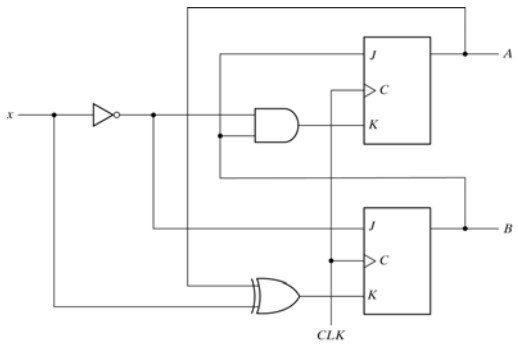


Fig. 5-18 Sequential Circuit with *JK* Flip-Flop

Input eqns:

$J_A = B$
$K_A = x'B$
$J_B = x'$
$K_B = x \text{ XOR } A$

JK-FF Example (2)

Input eqns:

$J_A = B$
$K_A = x'B$
$J_B = x'$
$K_B = x \text{ XOR } A$

Present State		Input	Next State		FF Inputs			
A	B	x	A	B	J_A	K_A	J_B	K_B
0	0	0			0	0	1	0
0	0	1			0	0	0	1
0	1	0			1	1	1	0
0	1	1			1	0	0	1
1	0	0			0	0	1	1
1	0	1			0	0	0	0
1	1	0			1	1	1	1
1	1	1			1	0	0	0

JK-FF Example (3)

Input eqns:

$J_A = B$
$K_A = x'B$
$J_B = x'$
$K_B = x \text{ XOR } A$

Characteristic Table

J	K	Q(t+1)	
0	0	Q(t)	
0	1	0	"Reset"
1	0	1	"Set"
1	1	Q'(t)	"Complement"

Present State A	B	Input x	Next State A	B	FF Inputs J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

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JK-FF Example (3)

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Present State A	B	Input x	Next State A	B	FF Inputs J_A	K_A	J_B	K_B
0	0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	0	1
0	1	0	1	1	1	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	1	1	0	0	1	1
1	0	1	1	0	0	0	0	0
1	1	0	0	0	1	1	1	1
1	1	1	1	1	1	0	0	0

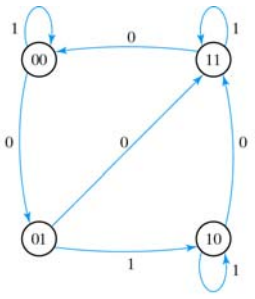

Fig. 5-19 State Diagram of the Circuit of Fig. 5-18

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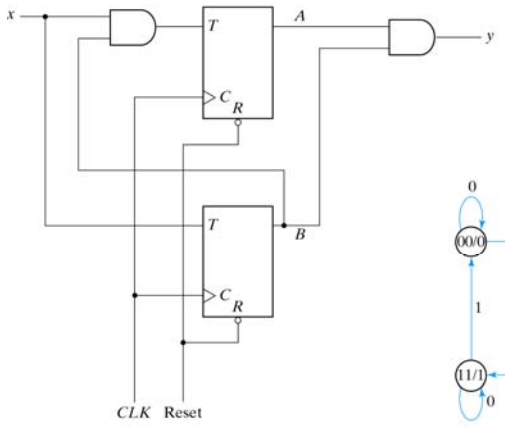
T-FF Example



Characteristic Table

T	Q(t+1)
0	Q(t)
1	Q'(t)

(a) Circuit diagram (b) State diagram

Fig. 5-20 Sequential Circuit with *T* Flip-Flops

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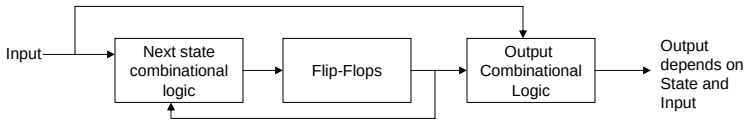
Mealy and Moore Designs

Mealy Machine



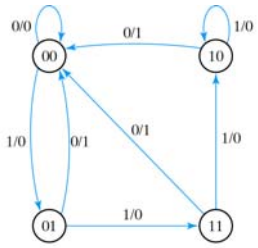


Fig. 5-16 State Diagram of the Circuit of Fig. 5-15

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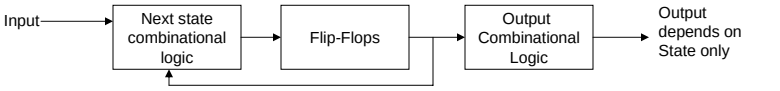
Mealy and Moore Designs

Moore Machine



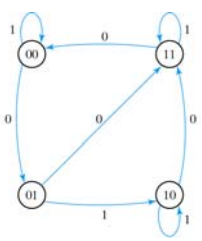
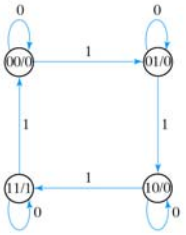


Fig. 5-19 State Diagram of the Circuit of Fig. 5-18



(b) State diagram

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Sequential Circuit Synthesis

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Synthesis procedure

1. Draw the state diagram
2. Assign binary codes to the states
3. Build the state table
4. Decide on FF types and write the FF input equations
5. Draw the logic diagram

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"111…" sequence detector

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Design a circuit that detects a sequence of 3 or more consecutive 1's

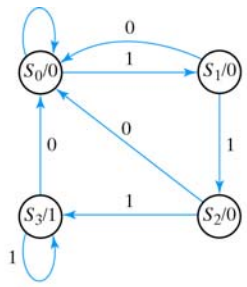

Fig. 5-24 State Diagram for Sequence Detector

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Assign binary codes to the states

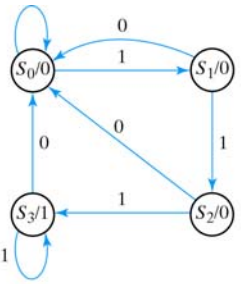

Fig. 5-24 State Diagram for Sequence Detector

	A	B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

Note that there are other ways to make this assignment

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Build the state table

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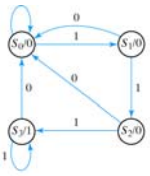

Fig. 5-24 State Diagram for Sequence Detector

	A	B
S0	0	0
S1	0	1
S2	1	0
S3	1	1

Present State A	Present State B	Input x	Next State A	Next State B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

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Determine FF Types and write the FF input equations

Say we use D-FF's

Present State A	B	Input x	Next State A	B	Output y
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	1	1	0
1	1	0	0	0	1
1	1	1	1	1	1

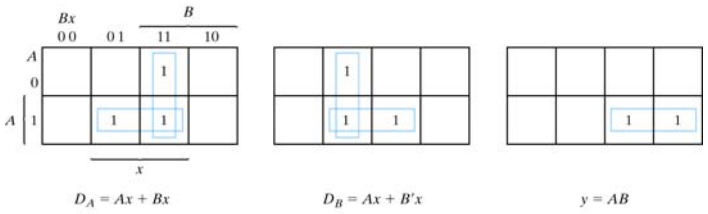

Fig. 5-25 Maps for Sequence Detector

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Draw the logic diagram

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DA = Ax + Bx
DB = Ax + B'x
y=AB

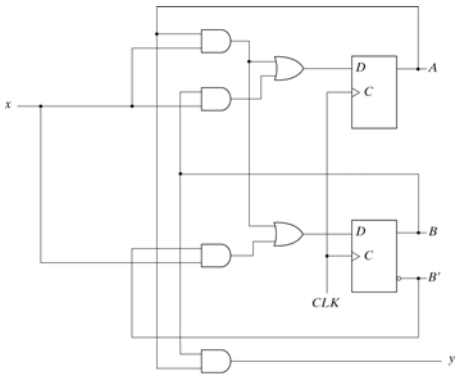

Fig. 5-26 Logic Diagram of Sequence Detector

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Making it easier to develop FF Input Equations

The "Excitation Table"

D-FF

Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

JK-FF

Q(t)	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

T-FF

Q(t)	Q(t+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

KNOW THESE!

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A JK-FF Example (1)

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State Table

Present State A	Present State B	Input x	Next State A	Next State B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

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A JK-FF Example (2)

State Table

Present State A	Present State B	Input x	Next State A	Next State B
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

JK Excitation Table

Q(t)	Q(t+1)	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

State Table with FF Inputs

Present State A	Present State B	Input x	Next State A	Next State B	FF Inputs JA	KA	JB	KB
0	0	0	0	0	0	d	0	d
0	0	1	0	1	0	d	1	d
0	1	0	1	0	1	d	d	1
0	1	1	0	1	0	d	d	0
1	0	0	1	0	d	0	0	d
1	0	1	1	1	d	0	1	d
1	1	0	1	1	d	0	d	0
1	1	1	0	0	d	1	d	1

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A JK-FF Example (3)

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Present State A	Present State B	Input x	Next State A	Next State B	FF Inputs JA	KA	JB	KB
0	0	0	0	0	0	d	0	d
0	0	1	0	1	0	d	1	d
0	1	0	1	0	1	d	d	1
0	1	1	0	1	0	d	d	0
1	0	0	1	0	d	0	0	d
1	0	1	1	1	d	0	1	d
1	1	0	1	1	d	0	d	0
1	1	1	0	0	d	1	d	1

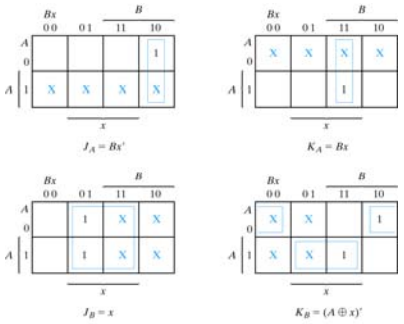

Fig. 5-27 Maps for J and K Input Equations

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A JK-FF example (4)

$J_A = Bx'$
$K_A = Bx$
$J_B = x$
$K_B = (A \text{ XOR } x)'$

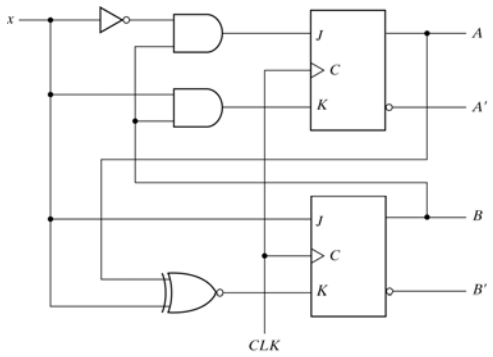

Fig. 5-28 Logic Diagram for Sequential Circuit with *JK* Flip-Flops

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A simple binary counter

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State diagram, state table, FF inputs

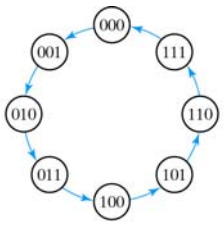

Fig. 5-29 State Diagram of 3-Bit Binary Counter

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For T Flip Flops

PS			NS			FF inputs		
A_2	A_1	A_0	A_2	A_1	A_0	T_{A2}	T_{A1}	T_{A0}
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Use K-Maps to determine:

$T_{A2} = A_1A_0$
$T_{A1} = A_0$
$T_{A0} = 1$

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Circuit

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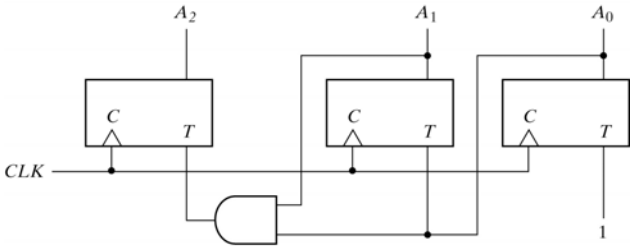

Fig. 5-31 Logic Diagram of 3-Bit Binary Counter

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