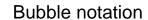
# Sections 3.7-3.9 Combinational Circuit Implementation

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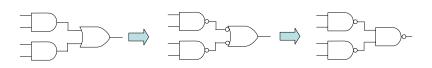
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To keep diagrams simple, we can represent the complement operation with just the circle part of the inverter gate.

Among other things, this helps us visualize ways to convert between gate types:

$$y - c$$
  $y - c$   $x'y' = (x+y)'$   $y$   $y - c$ 

$$x \longrightarrow x' + y' = (xy)' \longrightarrow x \longrightarrow y$$



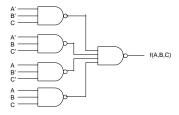
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## Review - 2-level NAND implementations

We can go directly from an SOP expression to a 2-level NAND circuit

f(ABC) = A'B'C + A'BC' + AB'C' + ABC



Note that a 2-level implementation does not necessarily use the minimum number of gates, nor can we constrain the number of inputs to the gates

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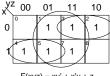
### General process for 2-level NAND circuits

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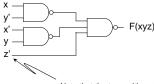
- 1. Simplify the function into SOP form
- 2. Use a first-level NAND for each term that has at least 2 literals
- 3. Use a second-level NAND to combine all terms
- 4. Invert any term with one literal in the first level.

Example 3.10

 $F(xyz) = \Sigma m(1-7)$ 

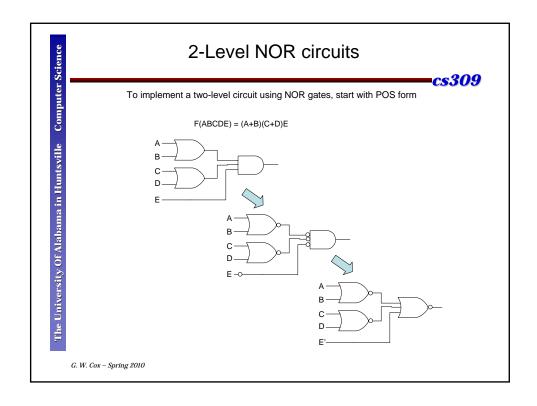


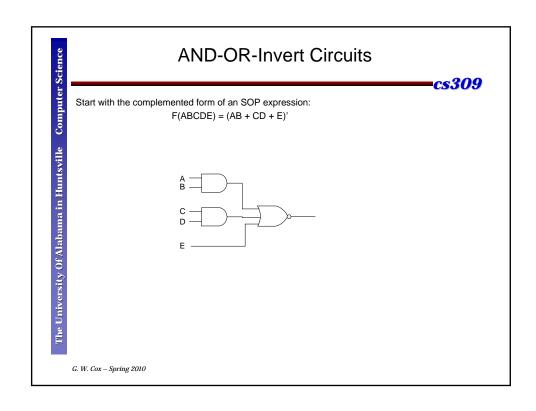
F(xyz) = xy' + x'y + z

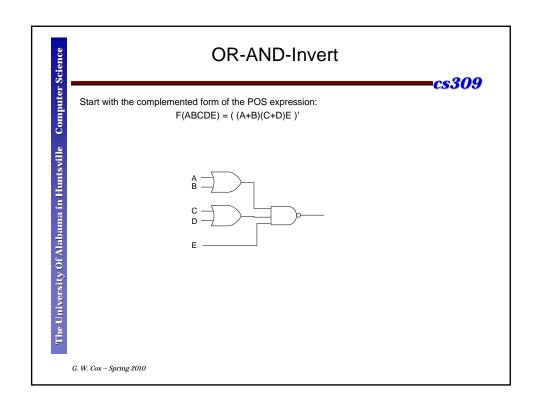


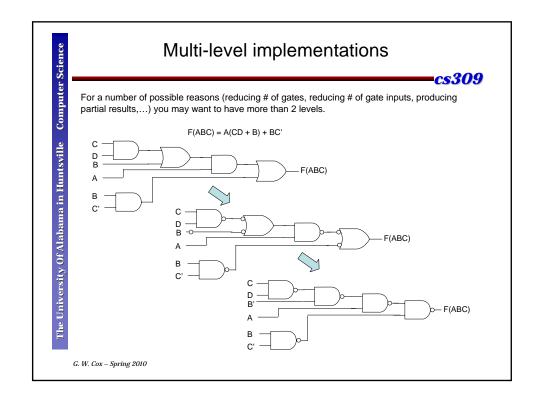
Note that the term with a single literal has to be complemented.

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#### XOR gates - review

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• A XOR B = AB' + A'B

Some characteristics:

- x XOR 0 = x
- x XOR 1 = x'
- x XOR x = 0
- x XOR x' = 1
- x XOR y' = x' XOR y = (x XOR y)'
- XOR implements the "odd" function:

a XOR b XOR c XOR ... = 1 IFF an odd # of (a,b,c,...) equals 1

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#### XORs in Parity Encoding

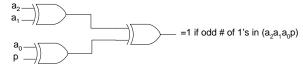
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- Recall that we can add a "parity bit" to a data item that lets us detect some errors
  - "odd parity" == set the parity bit so that the overall # of 1's is odd
  - "even parity" == set the parity bit so that the overall # of 1's is even

Even parity generator for 3-bit data

$$a_2$$
 $a_1$ 
 $a_0$ 
 $p = parity bit for even parity$ 

Even parity checker for 3-bit data



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