CS309 Spring 2010 Midterm Exam 2 Name _____

Except where otherwise stated, you may use any type of logic gates in your design. You can assume that there are no restrictions on the number of inputs to gates. Assume variables are available in both uncomplemented and complemented forms.

Neatness counts! If I can't read it, I can't give you credit for it.

SHOW ALL WORK.

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1. (15 pts) Design a minimized NAND circuit that inputs a BCD digit adds 6 and outputs the result as a 4-bit binary number. Call the bits of the BCD input A, B, C, and D. Call the output bits w, x, y, and z. Show: (a) the truth table, (b) minimized SOP expressions, (c) circuit diagram.

2. (15 pts) A logic circuit inputs a 4-bit binary number and subtracts 1 from it. Call the bits of the input E, F, G, and H and call the output bits p, q, r, and s. Assume that ABCD is always one or greater. Design the circuit using 4 Full Adders and additional logic gates as required.

3. (10 pts) Design a priority encoder for 4 data lines, D_0-D_3. D_x has priority over D_y if $x > y$. Your circuit should include a Valid ("V") output such that V=1 if any of the data lines is 1. Show: (a) the truth table, (b) minimized SOP expressions, (c) circuit diagram.

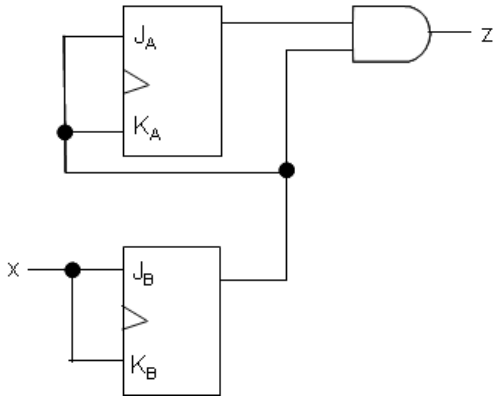
4. (10 pts) Use a 3x8 decoder and NOR gates to implement the function F(x,y,z) = xy + y'z + yz

5. (10 pts) Use an 8-input Multiplexer to implement the function
F(A,B.C.D) = A'B'D + AB + BC'D' + ACD.

6. (6 pts) Write the Characteristic Tables for: (a) D FF, (b) T FF, (c) JK FF

7. (6 pts) Write the Excitation Tables for: (a) D FF, (b) T FF, (c) JK FF

8. (13 pts) Draw the state diagram for the following circuit.



9. (15 pts) Design a sequence detector for the sequence 0101. Use D Flip-Flops in a Mealy design. Assume that there is no overlap between sequences (for example “01010101” is two occurrences of the sequence, not three). Show: (a) the state diagram, (b) state table, (c) minimized Boolean equations for the flip-flip inputs and circuit output, (d) circuit diagram.