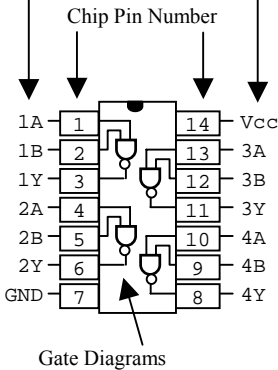
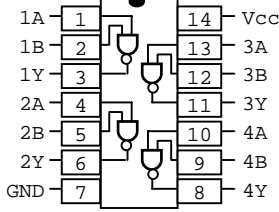
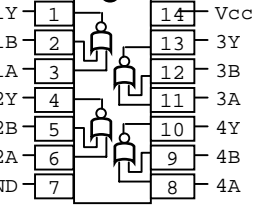
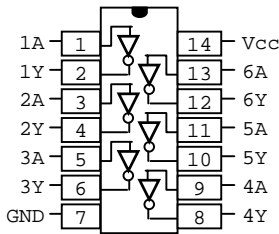


Valid Chips	Truth Table	Pin Diagram
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KEY		
<p>The numbers of chips that are identical in function for this lab appear here.</p>	<p>The Truth Table for the Gate(s) on the chip appears here.</p>	<p>A diagram of the chip appears here.</p> <p>Pin Type (Gate Number & Gate In/Output Identification)</p> 

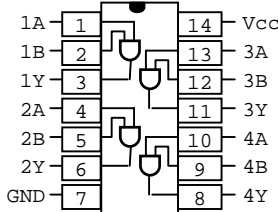
7400 Quadruple 2-Input NAND Gates																	
<p>N7400N N74H00N N74S00N N74LS00N N7400F N74H00F N74S00F N74LS00F</p>	<table border="1" data-bbox="682 955 974 1113"> <thead> <tr> <th>Input A</th> <th>Input B</th> <th>Output Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	Input A	Input B	Output Y	L	L	H	L	H	H	H	L	H	H	H	L	
Input A	Input B	Output Y															
L	L	H															
L	H	H															
H	L	H															
H	H	L															

7402 Quadruple 2-Input NOR Gates																	
<p>N7402N N74S02N N74LS02N N7402F N74S02F N74LS02F</p>	<table border="1" data-bbox="682 1253 974 1411"> <thead> <tr> <th>Input A</th> <th>Input B</th> <th>Output Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	Input A	Input B	Output Y	L	L	H	L	H	L	H	L	L	H	H	L	
Input A	Input B	Output Y															
L	L	H															
L	H	L															
H	L	L															
H	H	L															

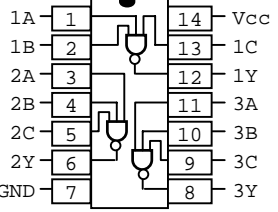
7404 Six Inverters								
<p>N7404N N74H04N N74S04N N74LS04N N7404F N74H04F N74S04F N74LS04F</p>	<table border="1" data-bbox="727 1539 928 1648"> <thead> <tr> <th>Input A</th> <th>Output Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> </tr> </tbody> </table>	Input A	Output Y	L	H	H	L	
Input A	Output Y							
L	H							
H	L							

Valid Chips	Truth Table	Pin Diagram
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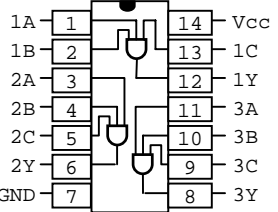
7408 Quadruple 2-Input AND Gates

N7408N	N74H08N	<table border="1"> <thead> <tr> <th>Input</th> <th>Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	Input	Input	Output	A	B	Y	L	L	L	L	H	L	H	L	L	H	H	H	
Input	Input		Output																		
A	B		Y																		
L	L		L																		
L	H		L																		
H	L	L																			
H	H	H																			
N74S08N	N74LS08N																				
N7408F	N74H08F																				
N74S08F	N74LS08F																				

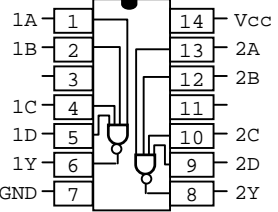
7410 Triple 3-Input NAND Gates

N7410N	N74H10N	<table border="1"> <thead> <tr> <th>Input</th> <th>Input</th> <th>Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	Input	Input	Input	Output	A	B	C	Y	L	L	L	H	L	L	H	H	L	H	L	H	L	H	H	H	H	L	L	H	H	L	H	H	H	H	L	H	H	H	H	L	
Input	Input		Input	Output																																							
A	B		C	Y																																							
L	L		L	H																																							
L	L		H	H																																							
L	H	L	H																																								
L	H	H	H																																								
H	L	L	H																																								
H	L	H	H																																								
H	H	L	H																																								
H	H	H	L																																								
N74S10N	N74LS10N																																										
N7410F	N74H10F																																										
N74S10F	N74LS10F																																										

7411 Triple 3-Input AND Gates

N7411N	N74H11N	<table border="1"> <thead> <tr> <th>Input</th> <th>Input</th> <th>Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>L</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>H</td> </tr> </tbody> </table>	Input	Input	Input	Output	A	B	C	Y	L	L	L	L	L	L	H	L	L	H	L	L	L	H	H	L	H	L	L	L	H	L	H	L	H	H	L	L	H	H	H	H	
Input	Input		Input	Output																																							
A	B		C	Y																																							
L	L		L	L																																							
L	L		H	L																																							
L	H	L	L																																								
L	H	H	L																																								
H	L	L	L																																								
H	L	H	L																																								
H	H	L	L																																								
H	H	H	H																																								
N74S11N	N74LS11N																																										
N7411F	N74H11F																																										
N74S11F	N74LS11F																																										

7420 Double 4-Input NAND Gates

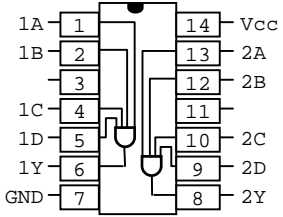
N7420N	N74H20N	<table border="1"> <thead> <tr> <th>Input</th> <th>Input</th> <th>Input</th> <th>Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> <th>D</th> <th>Y</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>L</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>L</td> <td>H</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>L</td> <td>H</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>L</td> <td>H</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>L</td> <td>H</td> </tr> <tr> <td>H</td> <td>H</td> <td>H</td> <td>H</td> <td>L</td> </tr> </tbody> </table>	Input	Input	Input	Input	Output	A	B	C	D	Y	L	L	L	L	H	L	L	L	H	H	L	L	H	L	H	L	L	H	H	H	L	H	L	L	H	L	H	L	H	H	L	H	H	L	H	L	H	H	H	H	H	L	L	L	H	H	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H	H	L	
Input	Input		Input	Input	Output																																																																																								
A	B		C	D	Y																																																																																								
L	L		L	L	H																																																																																								
L	L		L	H	H																																																																																								
L	L		H	L	H																																																																																								
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L	H		L	L	H																																																																																								
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H	L		H	H	H																																																																																								
H	H	L	L	H																																																																																									
H	H	L	H	H																																																																																									
H	H	H	L	H																																																																																									
H	H	H	H	L																																																																																									
N74S20N	N74LS20N																																																																																												
N7420F	N74H20F																																																																																												
N74S20F	N74LS20F																																																																																												

Valid Chips	Truth Table	Pin Diagram
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7421 Double 4-Input AND Gates

N7421N N74H21N
N74LS21N
N7421F N74H21F
N74LS21F

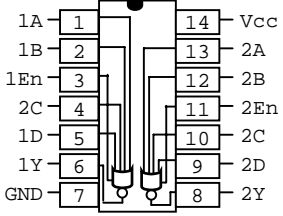
Input A	Input B	Input C	Input D	Output Y
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	H



7425 Double 4-Input NOR Gates w/Enable

N7425N
N7425F

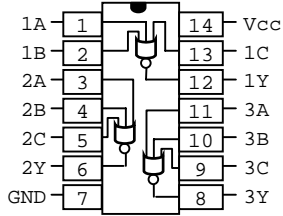
Input A	Input B	Input C	Input D	Output Y
L	L	L	L	H
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L



7427 Triple 3-Input NOR Gates

N7427N N74LS27N
N7427F N74LS27F

Input A	Input B	Input C	Output Y
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L



Valid Chips	Truth Table	Pin Diagram
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7430 8-Input NAND Gate

N7430N
N74H30N
N74LS30N
N7430F
N74H30F
N74LS30F

Input	Input	Input	Input	Input	Input	Input	Input	Input	Output
A	B	C	D	E	F	G	H	H	Y
All Other Cases									H

7432 Quadruple 2-Input OR Gates

N7432N N74H32N
N74S32N N74LS32N
N7432F N74H32F
N74S32F N74LS32F

Input	Input	Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

7473 Dual JK Master-Slave Flip-Flop

N7473N N74H73N
N74LS73N N7473F
N74H73F N74LS73F

Input	Input	Clear	Output	Output
J	K		Q(t+1)	Q'(t+1)
X	X	0	0	1
0	0	1	Q(t)	Q'(t)'
0	1	1	0	1
1	0	1	1	0
1	1	1	Q(t)'	Q(t)
Q(t)	Input	Input	Output	Output
	J	K	Q(t+1)	Q'(t+1)
0	0	X	0	1
0	1	X	1	0
1	X	1	0	1
1	X	0	1	0

X = Don't Cares

Note: In order for this flip-flop to work, clock should start low, transition to high, and then back to low while all inputs remain the same.

7483 4-Bit Full Adder

N7483N N74LS83N
N7483F N74LS83F

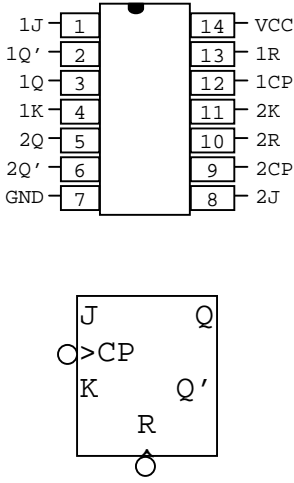
Carry	Input	Input	Output	Output
C_i	A_i	B_i	Σ_i	C_{i+1}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

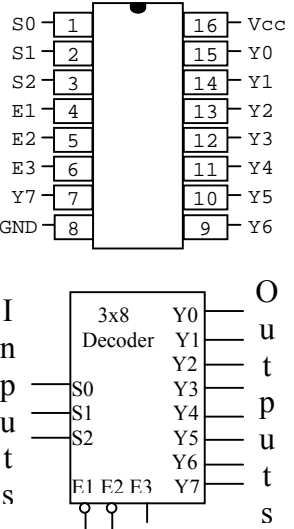
$i=0$ through 3

Note: C_{in} should be set to

Valid Chips	Truth Table	Pin Diagram
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	low when no carry in is intended and 1 when subtracting.	
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74107 Dual JK Master-Slave Flip-Flop																																																									
N74107N N74LS107N N74107F N74LS107F	<table border="1" data-bbox="613 636 1040 1003"> <thead> <tr> <th>Input J</th> <th>Input K</th> <th>Clear</th> <th>Output Q(t+1)</th> <th>Output Q'(t+1)</th> </tr> </thead> <tbody> <tr><td>X</td><td>X</td><td>0</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>Q(t)</td><td>Q(t)'</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>Q(t)'</td><td>Q(t)</td></tr> <tr> <th>Q(t)</th> <th>Input J</th> <th>Input K</th> <th>Output Q(t+1)</th> <th>Output Q'(t+1)</th> </tr> <tr><td>0</td><td>0</td><td>X</td><td>0</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>X</td><td>1</td><td>0</td></tr> <tr><td>1</td><td>X</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>X</td><td>0</td><td>1</td><td>0</td></tr> </tbody> </table> <p data-bbox="727 978 927 1003">X = Don't Cares</p> <p data-bbox="581 1010 1073 1220">Note: In order for this flip-flop to work, clock should start low, transition to high, and then back to low while all inputs remain the same.</p>	Input J	Input K	Clear	Output Q(t+1)	Output Q'(t+1)	X	X	0	0	1	0	0	1	Q(t)	Q(t)'	0	1	1	0	1	1	0	1	1	0	1	1	1	Q(t)'	Q(t)	Q(t)	Input J	Input K	Output Q(t+1)	Output Q'(t+1)	0	0	X	0	1	0	1	X	1	0	1	X	1	0	1	1	X	0	1	0	
Input J	Input K	Clear	Output Q(t+1)	Output Q'(t+1)																																																					
X	X	0	0	1																																																					
0	0	1	Q(t)	Q(t)'																																																					
0	1	1	0	1																																																					
1	0	1	1	0																																																					
1	1	1	Q(t)'	Q(t)																																																					
Q(t)	Input J	Input K	Output Q(t+1)	Output Q'(t+1)																																																					
0	0	X	0	1																																																					
0	1	X	1	0																																																					
1	X	1	0	1																																																					
1	X	0	1	0																																																					

74138 3X8 Decoder																																																																																																																
N74138N N74LS138N N74138F N74LS138F	<table border="1" data-bbox="565 1297 1089 1560"> <thead> <tr> <th colspan="3">Input</th> <th colspan="8">Output</th> </tr> <tr> <th>S0</th> <th>S1</th> <th>S2</th> <th>Y0</th> <th>Y1</th> <th>Y2</th> <th>Y3</th> <th>Y4</th> <th>Y5</th> <th>Y6</th> <th>Y7</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td></tr> </tbody> </table> <p data-bbox="586 1566 1068 1665">Note: E1 & E2 are active low enable. E3 is active high enable</p>	Input			Output								S0	S1	S2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1	0	1	1	1	1	1	1	0	1	0	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	0	1	1	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	
Input			Output																																																																																																													
S0	S1	S2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7																																																																																																						
0	0	0	0	1	1	1	1	1	1	1																																																																																																						
0	0	1	1	0	1	1	1	1	1	1																																																																																																						
0	1	0	1	1	0	1	1	1	1	1																																																																																																						
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1	1	0	1	1	1	1	1	1	0	1																																																																																																						
1	1	1	1	1	1	1	1	1	1	0																																																																																																						

Valid Chips	Truth Table	Pin Diagram
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74148 3X8 Encoder

N74148N N74148F

Output			Input							
Y0	Y1	Y2	I0	I1	I2	I3	I4	I5	I6	I7
0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1
0	1	0	1	1	0	1	1	1	1	1
0	1	1	1	1	1	0	1	1	1	1
1	0	0	1	1	1	1	0	1	1	1
1	0	1	1	1	1	1	1	0	1	1
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

Note: EI is active low enable. GS and EO are not used in this lab.

74151 8-Input Multiplexer

N74151N
N74S151N
N74LS151N
N74151F
N74S151F
N74LS151F

Select			Input								Output	
S0	S1	S2	I0	I1	I2	I3	I4	I5	I6	I7	Y	Y'
0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	X	0	X	X	X	X	X	X	0	1
0	0	1	X	1	X	X	X	X	X	X	1	0
0	1	0	X	X	0	X	X	X	X	X	0	1
0	1	0	X	X	1	X	X	X	X	X	1	0
0	1	1	X	X	X	0	X	X	X	X	0	1
0	1	1	X	X	X	1	X	X	X	X	1	0
1	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	X	X	X	X	X	0	X	X	0	1
1	0	1	X	X	X	X	X	1	X	X	1	0
1	1	0	X	X	X	X	X	0	X	0	0	1
1	1	0	X	X	X	X	X	1	X	1	0	0
1	1	1	X	X	X	X	X	X	0	0	0	1
1	1	1	X	X	X	X	X	X	1	1	0	0

X = Don't Cares

Note: E is active low enable.

74153 Dual 4-Input Multiplexer

N74153N N74S153N
N74LS153N N74153F
N74S153F
N74LS153F

Select			Input				Output
S0	S1	E'	I0	I1	I2	I4	Y
X	X	1	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
1	0	0	X	X	0	X	0
1	0	0	X	X	1	X	1
1	1	0	X	X	X	0	0
1	1	0	X	X	X	1	1

Valid Chips	Truth Table	Pin Diagram
	<div style="border: 1px solid black; padding: 2px; width: fit-content; margin: 0 auto;">X = Don't Cares</div> <p>Note: E is active low enable.</p>	